



NanolC

**Accelerating beyond-2nm
chip innovation across Europe**

Inge Asselberghs, imec

Co-funded by
 **ChipsJU**



NanoIC will provide Europe with a **beyond-2nm** leading edge system-on-chip pilot line.

It will develop advanced **logic**, novel **memories** and advanced **interconnect** technologies.

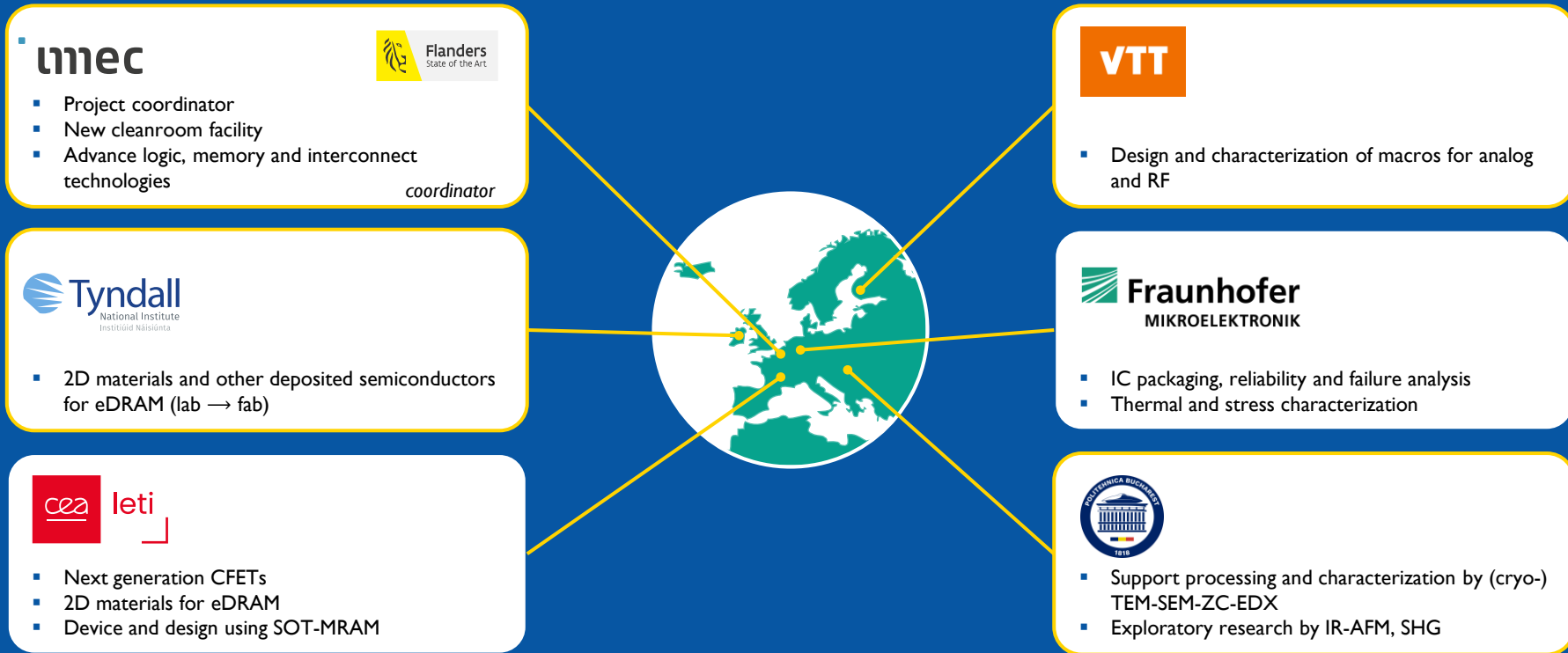
Infrastructure &
Equipment

Technology
development

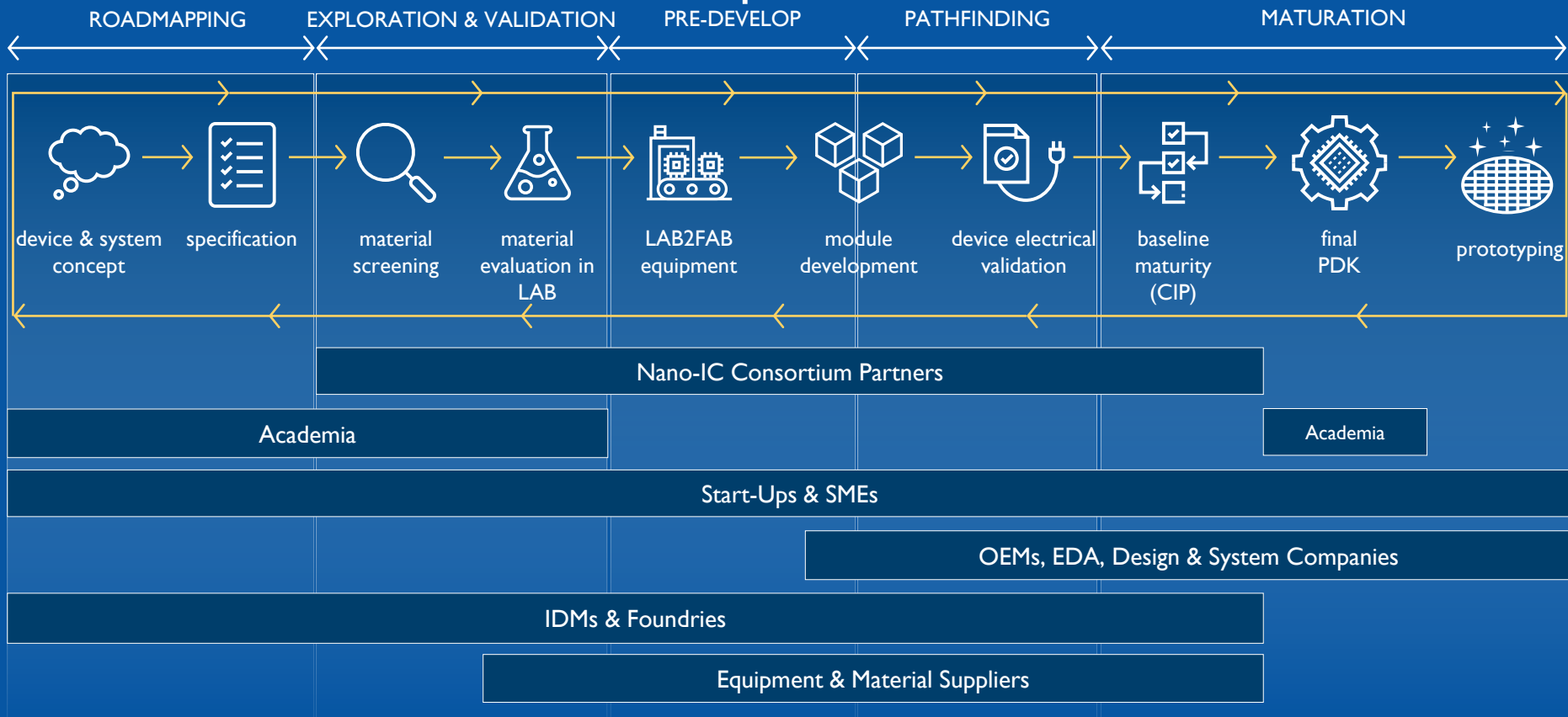
Access &
selection

Education & work
force
development

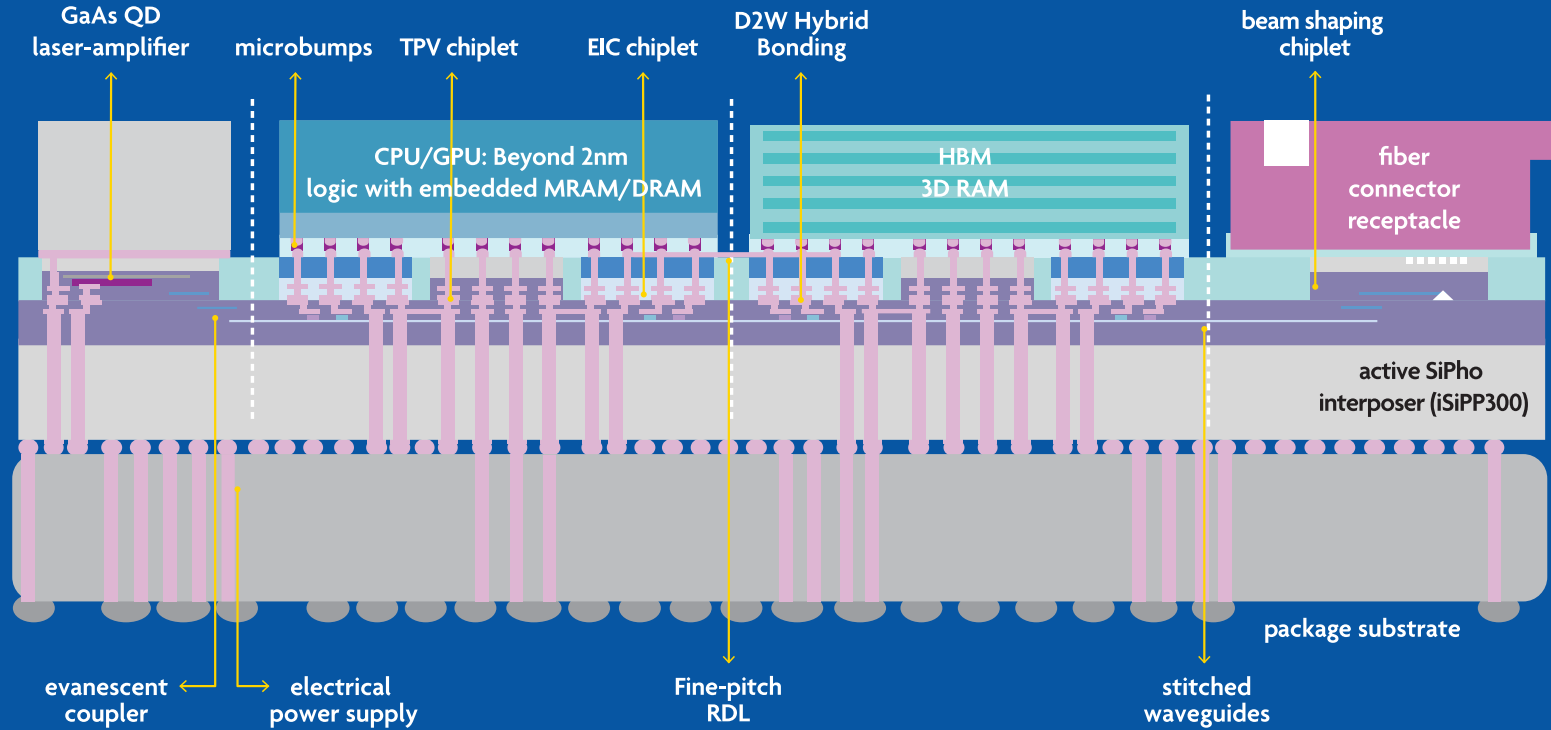
Meet the consortium



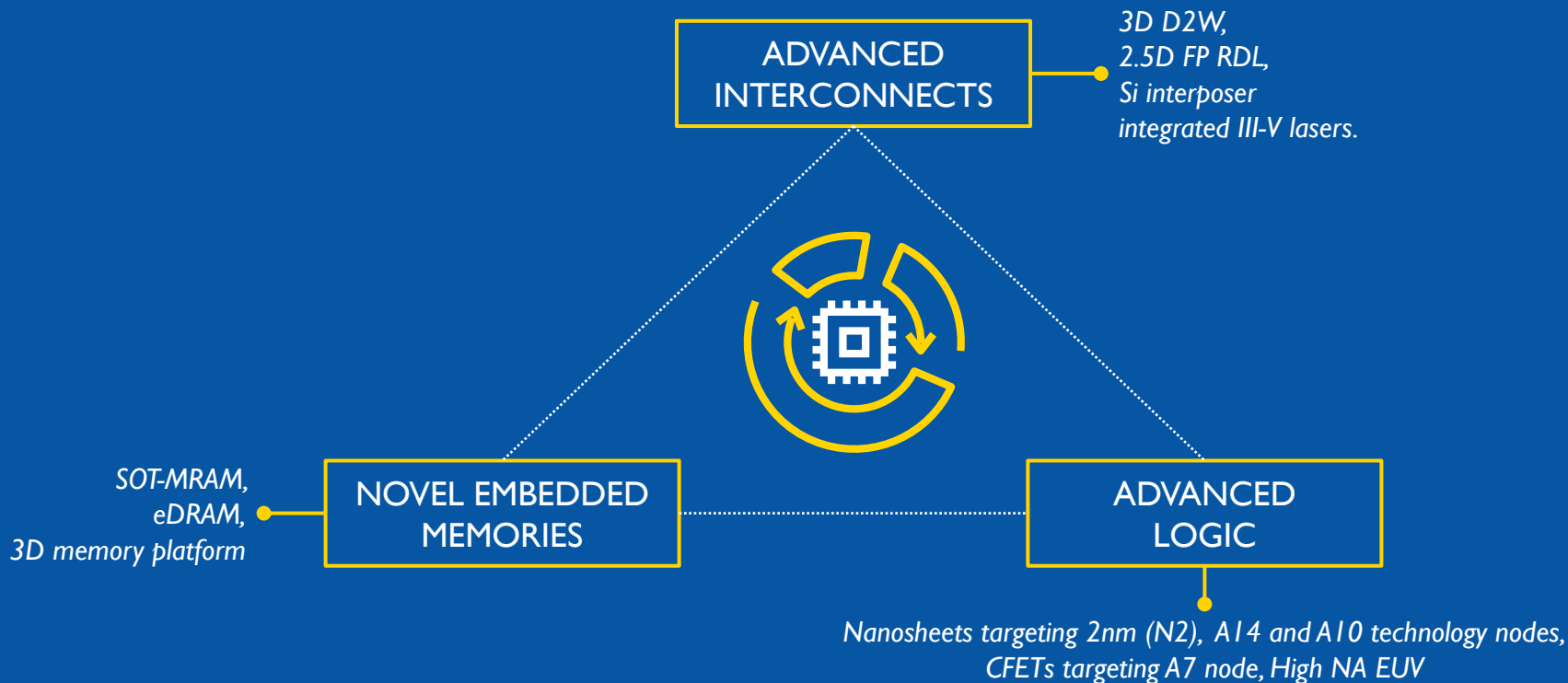
NanoIC activities within imec's pilot line



Future HPC system concept leveraging NanoIC technologies

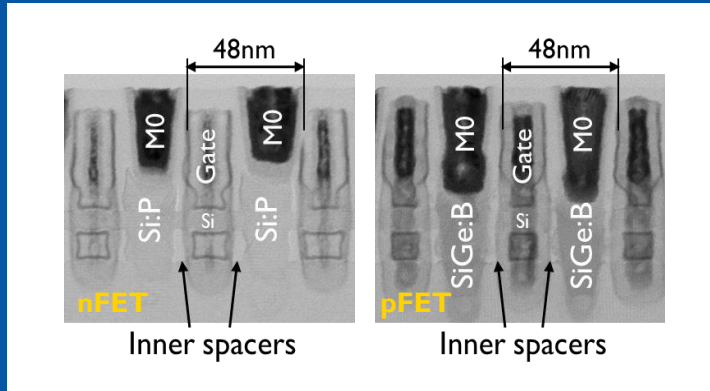


Technology platforms in NanoIC scope:

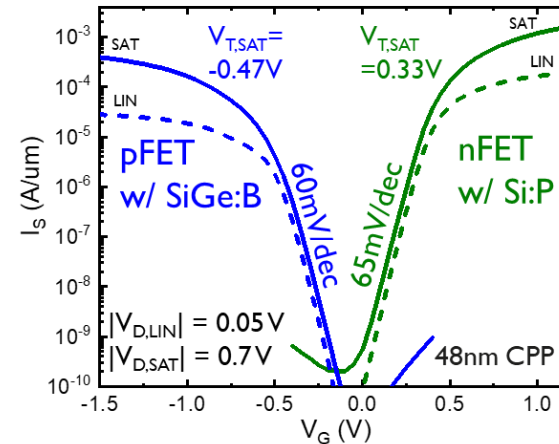


Advanced logic: nanosheet FET

- **Functional CMOS** demonstrated
- **Test Vehicle** → ready for further process and module exploration w material and tool suppliers
- Electrical result → **N2 research PDK**



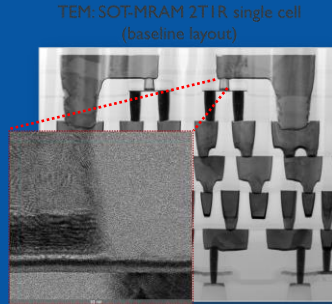
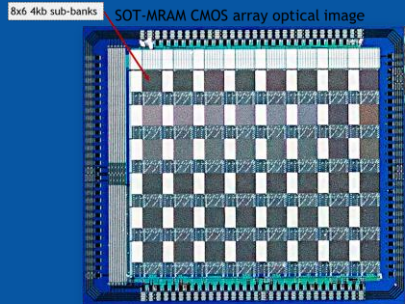
H. Arimura et.al. IEEE VLSI, 2024



Embedded memory macro for cache applications

SOT-MRAM

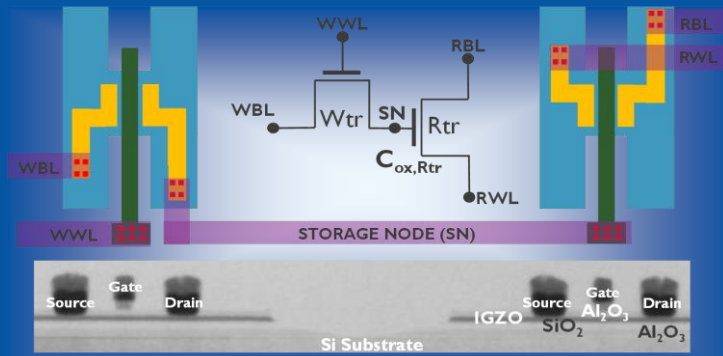
SOT-MRAM will be integrated
on 40nm CMOS technology



Latest results show excellent read/write
and retention (>10 yrs) properties

eDRAM

Latest results show excellent
retention achieved on side-by-side 2T0C*



Capacitorless eDRAM is now considered one the
most promising candidates for **AI applications**

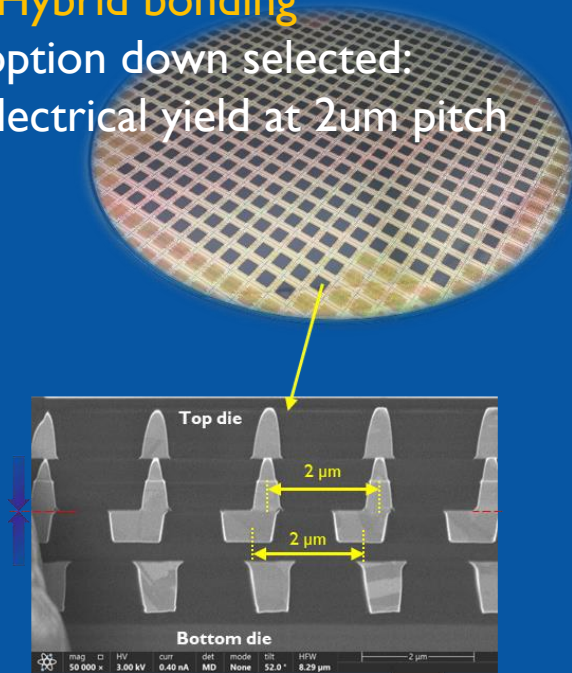
- **Upcoming:** availability of SOT eMRAM PDK and eDRAM PDK

Advanced interconnect: towards platform for prototyping

D2V Hybrid bonding

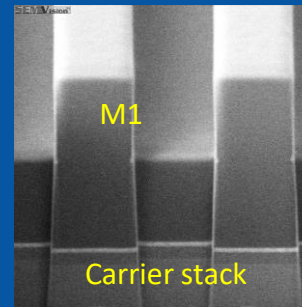
Flow option down selected:

1st electrical yield at 2 μ m pitch

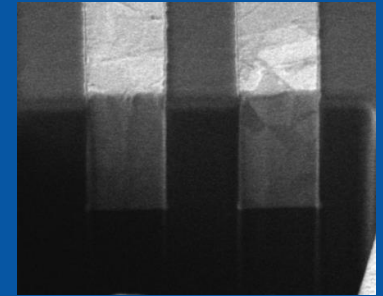


Fine pitch RDL

Enablement 1.3 μ m metal width interconnect



1.3 μ m L/S lithography

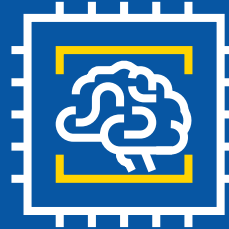


1.3 μ m L/S after CMP

To enable early exploration of developed technologies,
NanoIC offers:



DESIGN PATHFINDING
PDKs



SYSTEM EXPLORATION
PDKs

available to industry (including SMEs and start-ups) and academia

N2 PDK – Pathfinding PDK for future logic devices

An explorative design environment for 2nm Gate All Around (GAA) Transistors

The NanoIC project provides a comprehensive PDK environment for

- **designing,**
- **experimenting** with, and
- testing **innovative IC solutions** on advanced nodes.

The PDKs are **continuously benchmarked**

with physical devices (fabricated in imec's cleanrooms),

for maximum adherence to **realistic electrical behavior** of devices.

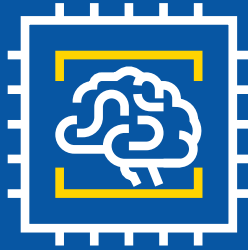


Free access

To build a skilled European semiconductor workforce,
the NanoIC pilot line offers:



PHDs



INTERNSHIPS



PDK WORKSHOPS



EXPERT COURSES

training

**N2 PATHFINDING PDK:
ADVANCED PDK WORKSHOP**

24-25 June, **IMEC** Leuven, Belgium

N2 PDK – Hands-on training

Extensive N2 PDK training to **engage directly with our R&D Team**

Next session: **24-25 June 2025**

- **Day 1:** Introduction to N2 Node and Open PDK:

- Process Integration,
- Standard Cell,
- Back-side Power Delivery Networks
- and more.

- **Day 2:** Hands-On EDA Tool Application



**Register
now**

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NanolC

The acquisition and operation of the NanolC pilot line are jointly funded by the Chips Joint Undertaking, through the European Union's Digital Europe (101183266) and Horizon Europe programs (101183277), as well as by the participating states Belgium (Flanders), France, Germany, Finland, Ireland and Romania.

Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.

Coordinated by **imec**

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Pilot line project partners

