FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

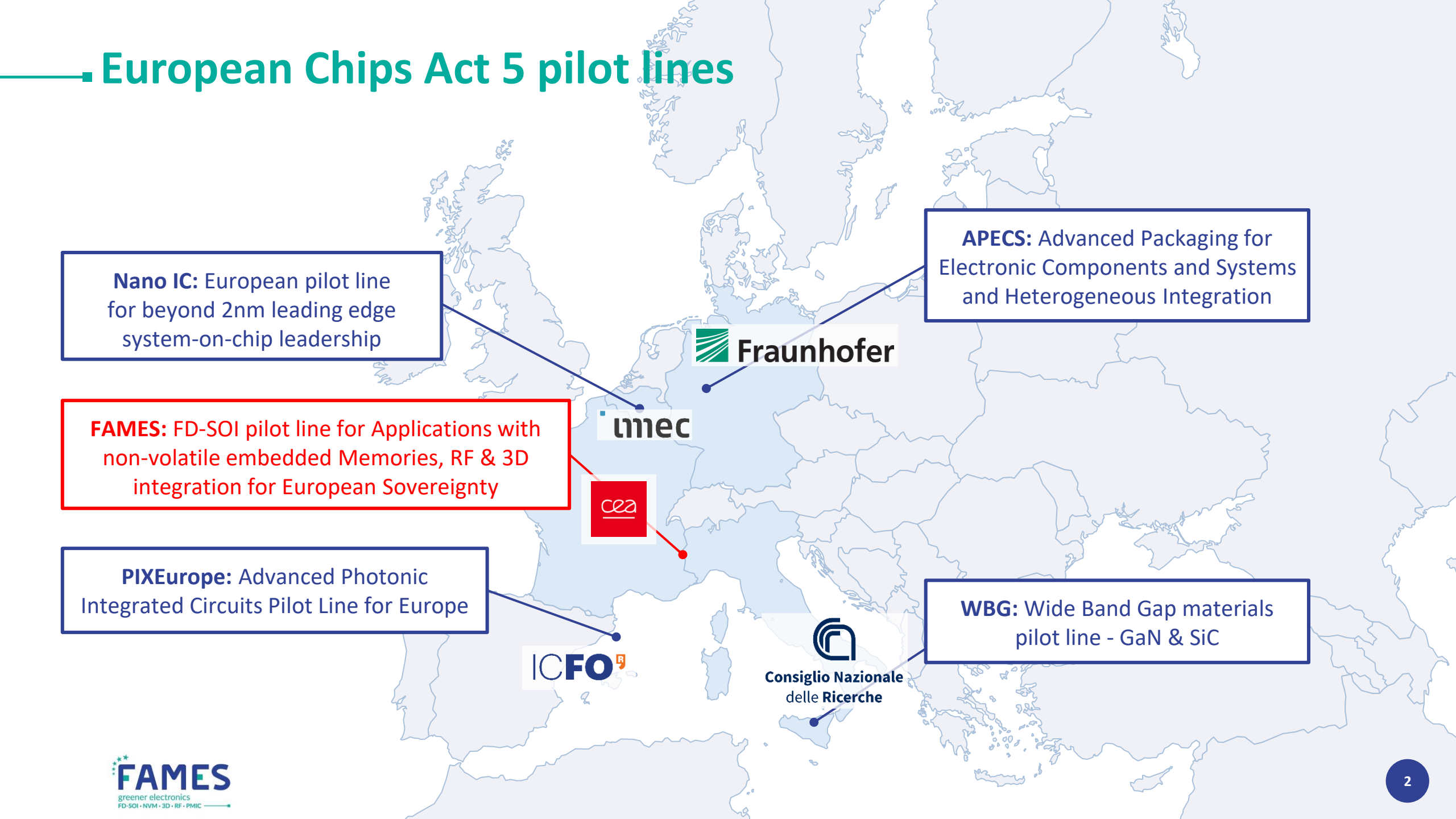
FAMES Pilot Line overview

Bavarian Semiconductor Conference, June 2nd, 2025

Bruno Paing, VP Europe & International Public Affairs – CEA-Leti (bruno.paing@cea.fr)

Chips JU

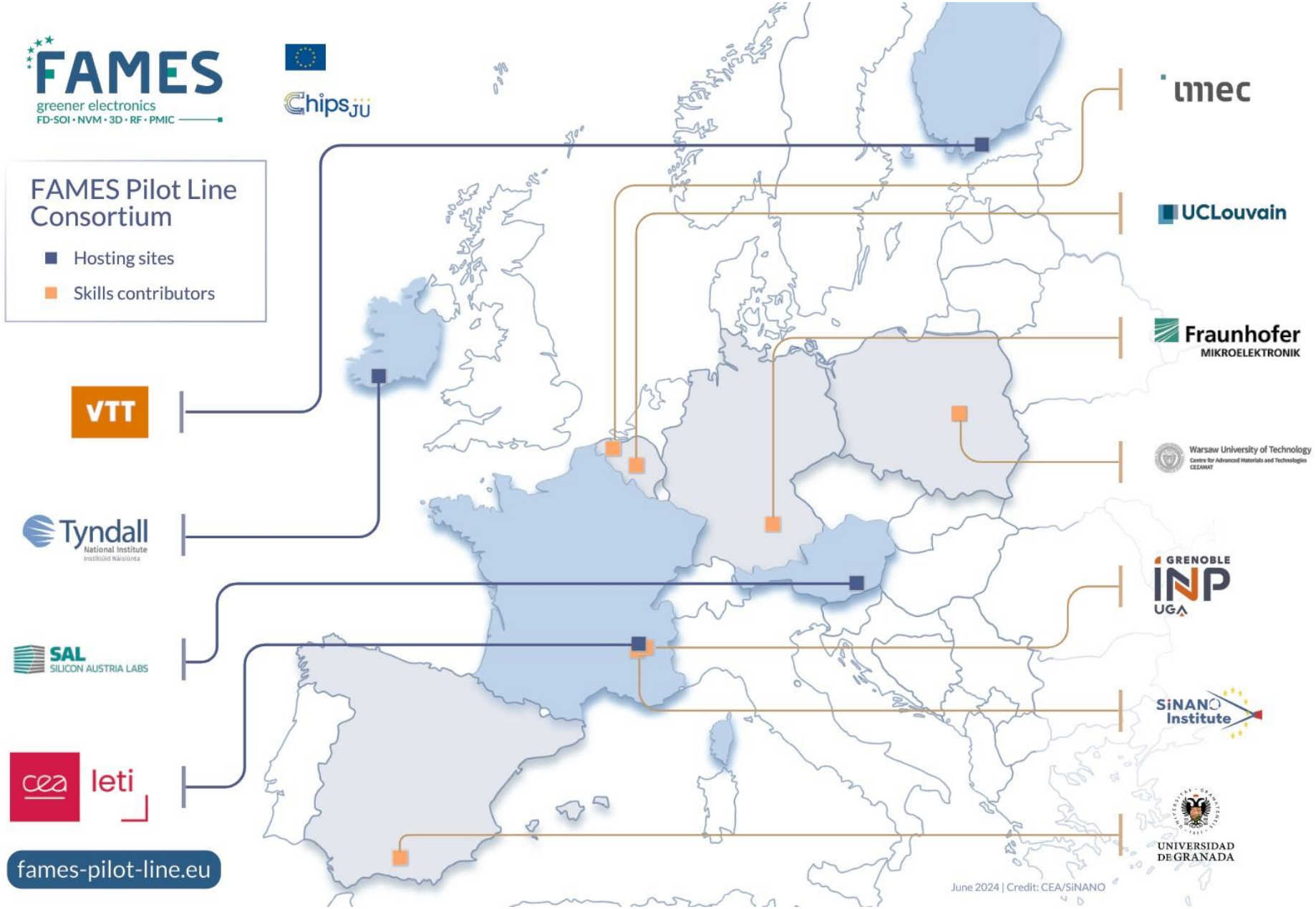
European Chips Act 5 pilot lines



FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

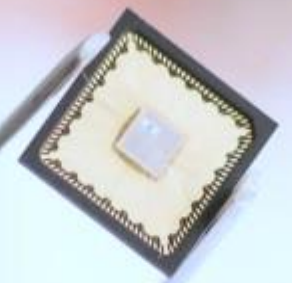
Budget : €830 M
- CAPEX: €382 M
- OPEX: €448 M

Funding mechanisms
- 50% Chips JU
- 50% Member States



Aim of FAMES

- A European semiconductor pilot line for advanced technologies
- With opportunities for disruptive chip architectures, performance improvements and significant energy savings
- Strengthening European leadership in advanced semiconductors and opening new economic opportunities for a wide spectrum of markets



Credits: Jayet/CEA

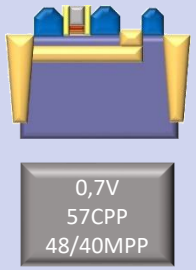
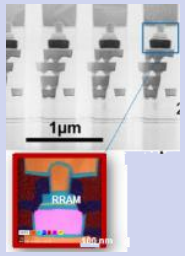
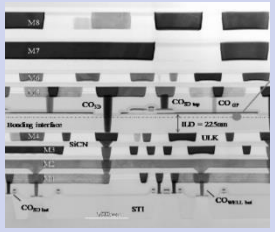
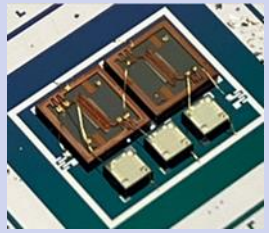
FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Opening the pilot line to European stakeholders

44 letters of support

FAMES Technology Portfolio

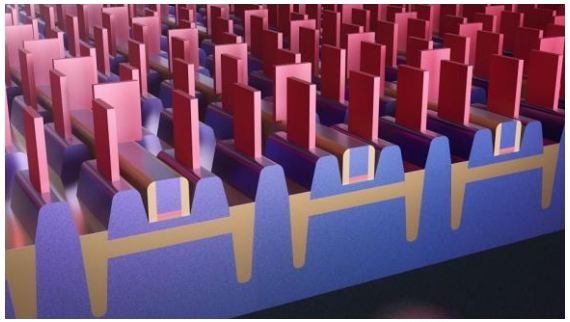
FAMES technological offer

FD-SOI	Embedded non-volatile memories	Radiofrequency components	3D integration	Small inductors for DC-DC converters	Eco-innovation
10 nm and 7 nm nodes 	OxRAM, FeRAM, MRAM and FeFET 	Switches, filters, and capacitors 	Heterogeneous and sequential 	Power management integrated circuits (PMIC) 	Evaluate and reduce environmental footprint   Environmental regulations
cea leti, imec, UCLouvain	cea leti, VTT, imec, UCLouvain, Fraunhofer, UNIVERSIDAD DE GRANADA	cea leti, VTT, SAL SILICON AUSTRIA LABS	cea leti, Tyndall National Institute	cea leti, Tyndall National Institute	cea leti, imec, cea list, UCLouvain

FD-SOI is the optimal PPAC-E (Power, Performance, Area, Cost, Environmental impact) trade-off for mixed-signals circuits

FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

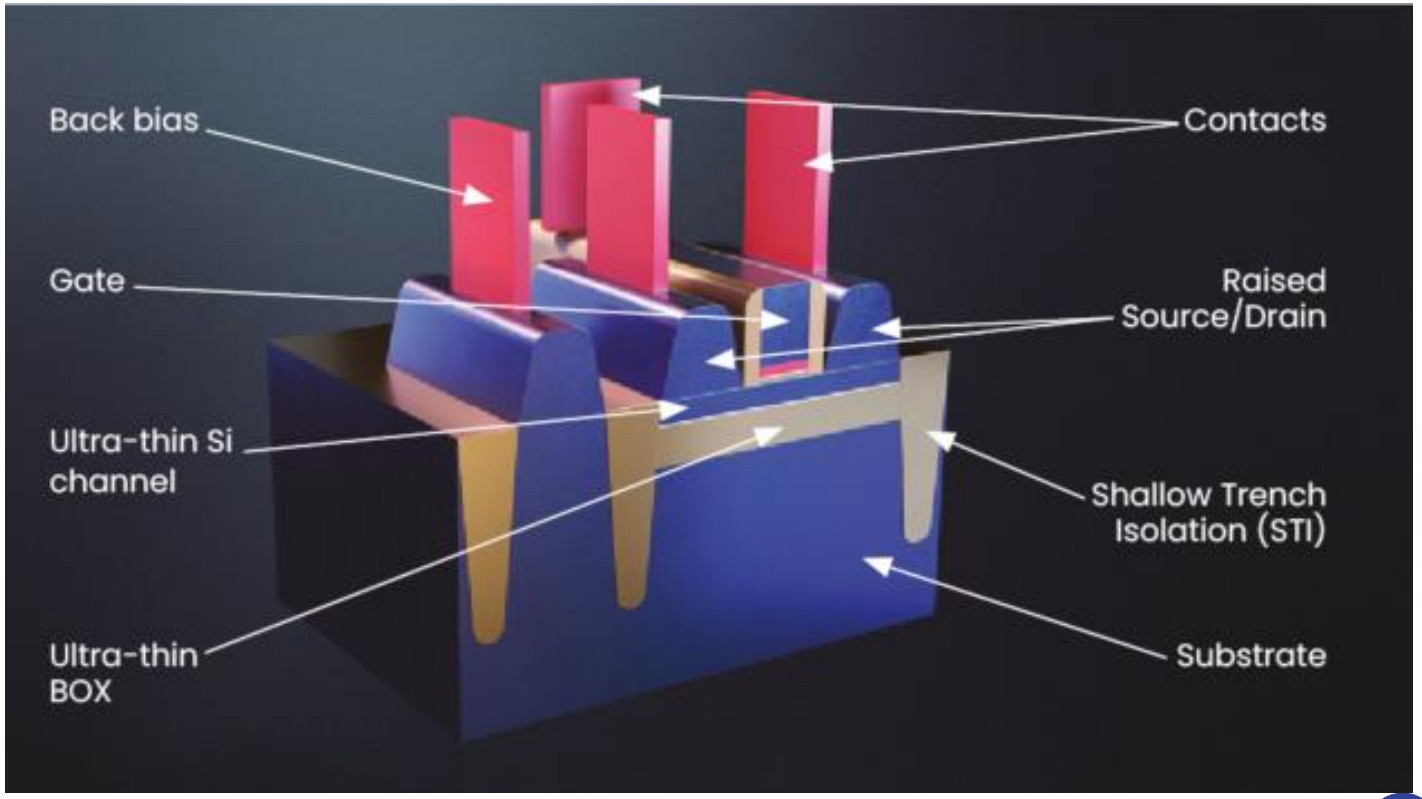
FD-SOI 10nm and 7nm nodes



An innovative generation of chips with the best balance in Power, Performance, Area, Cost and Environment (PPAC-E) for highly energy efficient applications

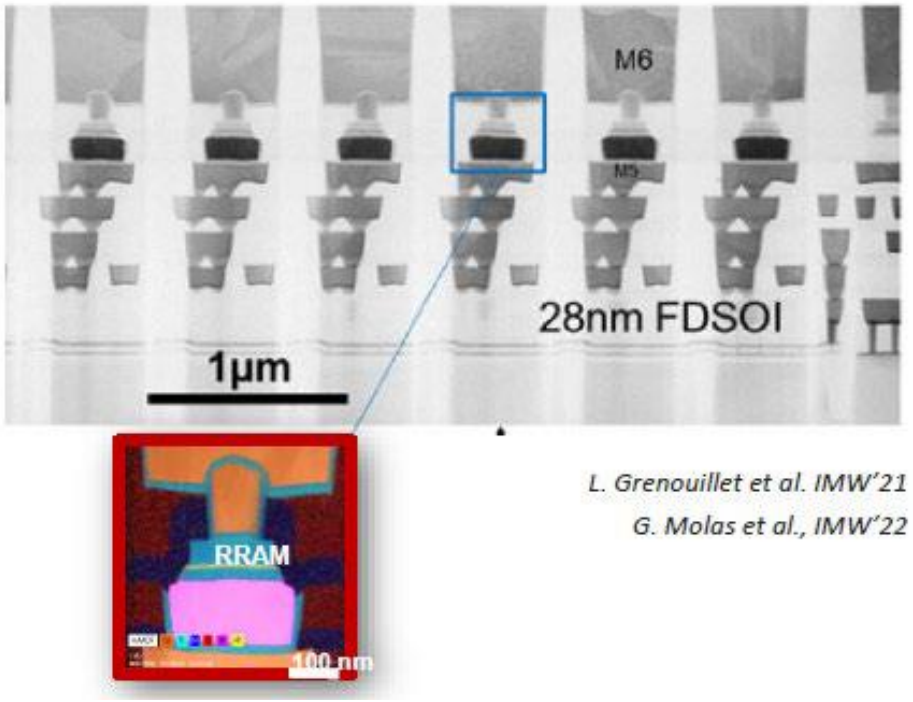
- Transistor density
- High-performance/low-power trade-off
- Radiation resistance
- Reduced current leakage
- Manufacturing costs

- Over **150 patents** filed by CEA-Leti



FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Emerging Non-Volatile Memories embedded in the BEOL



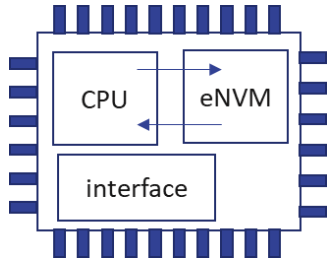
L. Grenouillet et al. IMW'21
G. Molas et al., IMW'22

EMBEDDED quicker access time and lower power compared to stand alone as they are on chip close to the logic

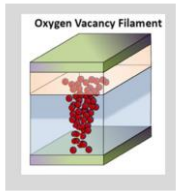
NON VOLATILE retaining data even when the power is off

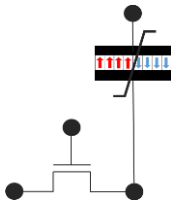
PERFORMANT reprogrammable and erasable multiple times, faster to write compared to Flash memories

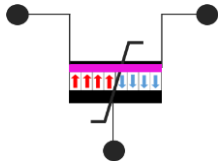
LOW POWER lower power consumption than external non volatile memories



OxRAM **MRAM** **FeRAM** **FeFET**





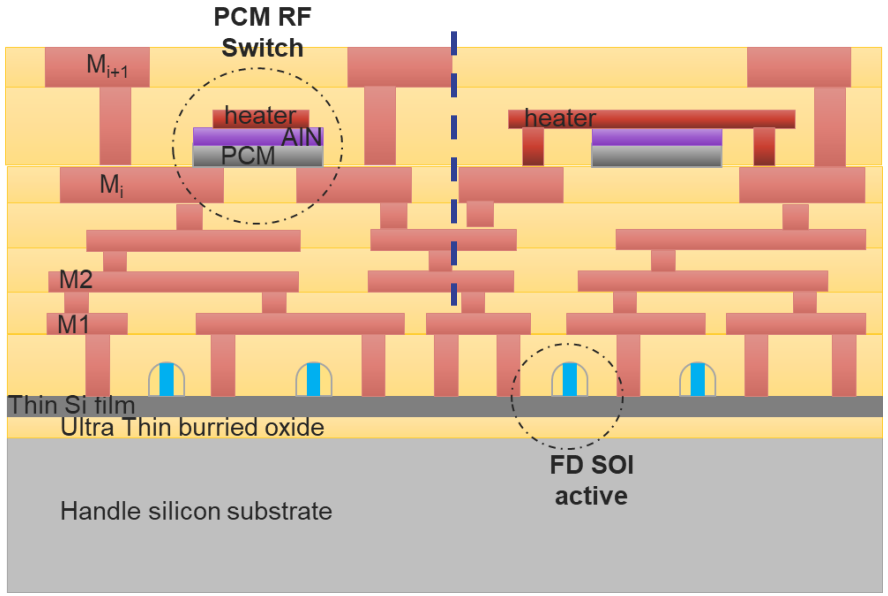


FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

RF components integrated in the BEOL

FD-SOI is well-suited for RF/analog and mixed signal circuits

- **Performance/power savings**
- **Covering a wide frequency range**
- **From a few GHz up to the D-band centered at 140 GHz**

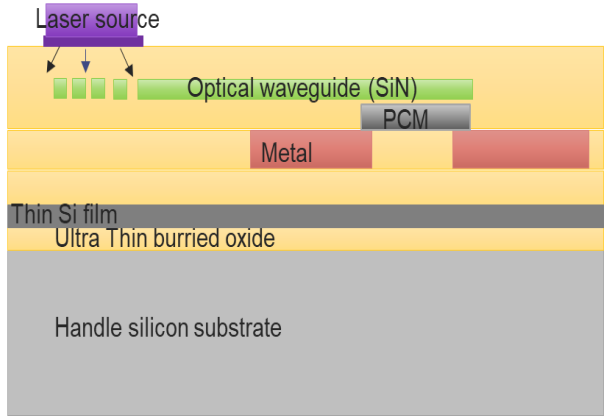


FAMES → RF active and **passive components**, to enrich the FD-SOI CMOS technology offer and open new markets:

- **RF switches based on Phase Change Materials**
- **RF acoustic filters**
- **RF magnetic-based miniaturized circulators for >GHz bands**

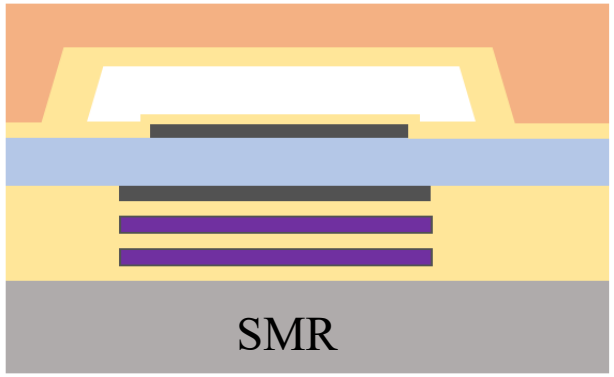
FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

RF switches and filters – integrated in the BEOL



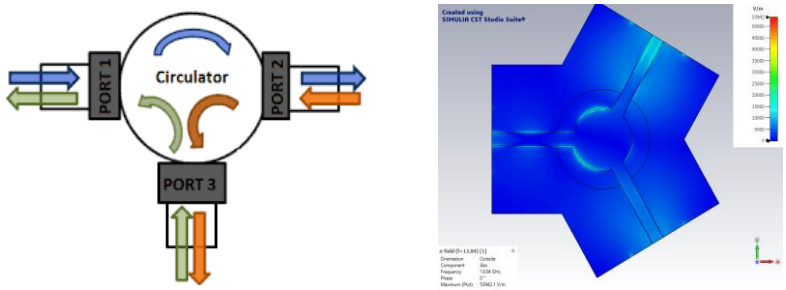
RF Switches based on PCM

- Optical actuator control - no interference from heater and biasing lines
- High performance switches > 100 GHz with Zero-static power consumption
- Lower insertion loss



RF Acoustic Filters

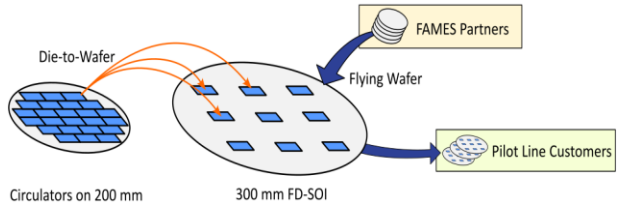
- BAW wide bandwidth filters in the 7-15 GHz range
- Single crystal piezoelectric thin films (LiNbO3 & AlScN)
- Acoustic & RF design of filter available via process design kit (PDK)



3-port Circulator schematic and FE-simulation

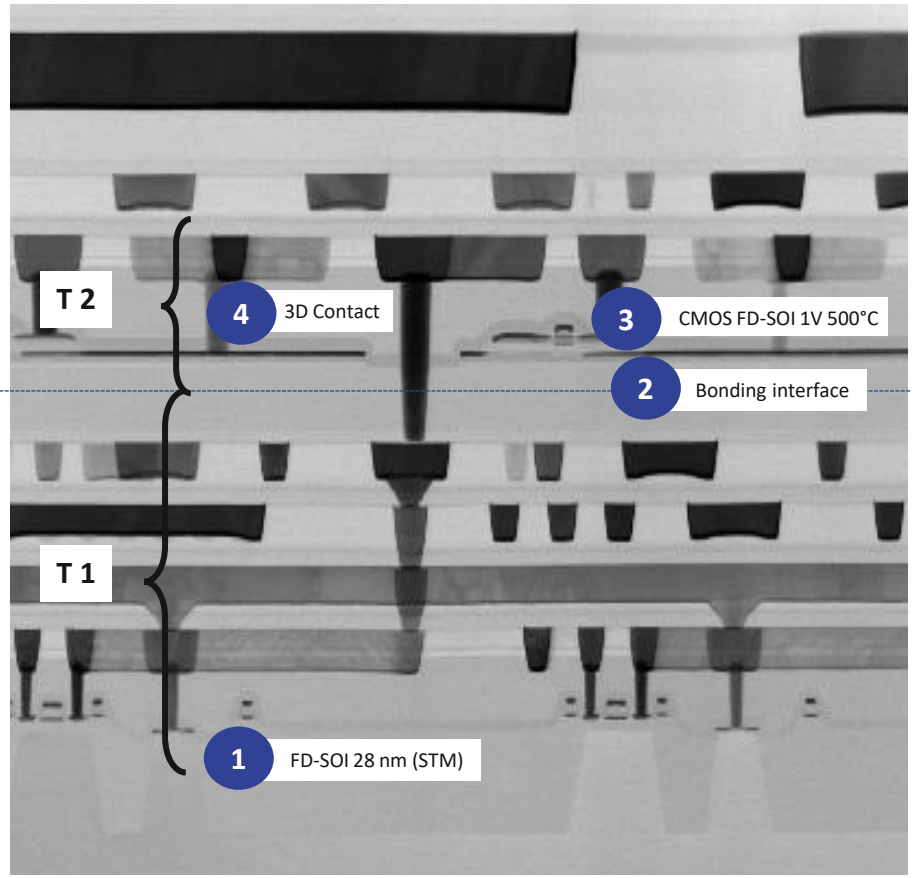
RF magnetic mini- circulators

- Self-biased circulators for FR3 /X bands and lower FR2/K bands
- Miniaturized, cost-efficient solution for effective signal routing
- PDK under development



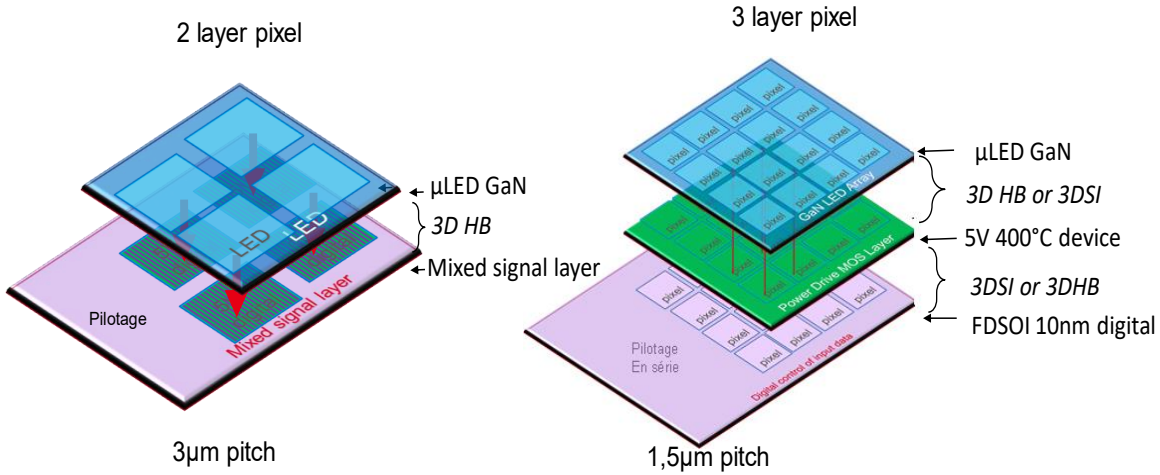
FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

3D Sequential integration



FAMES aims to enlarge FD-SOI heterogeneous co-integration with other devices using 3DSI to address new systems and markets

- Demonstrate 3D sequential integration with increasingly complex circuits;
- Evaluate opportunity of Smart and scaled 3tier-pixels with GaN µLED and RF applications



FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Heterogeneous Integration : technology development

New high density interconnects by direct hybrid bonding

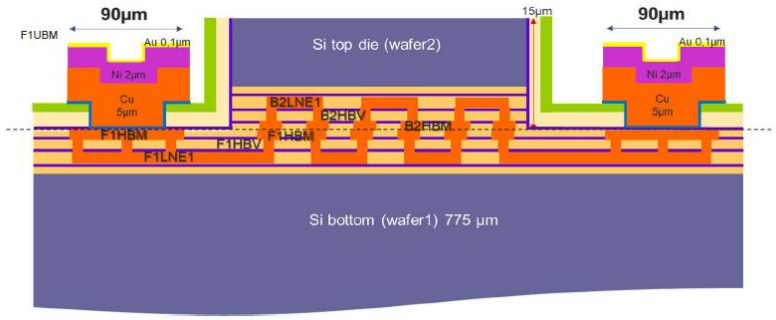
- Die-to-wafer implementation
- Pitch target below 1µm

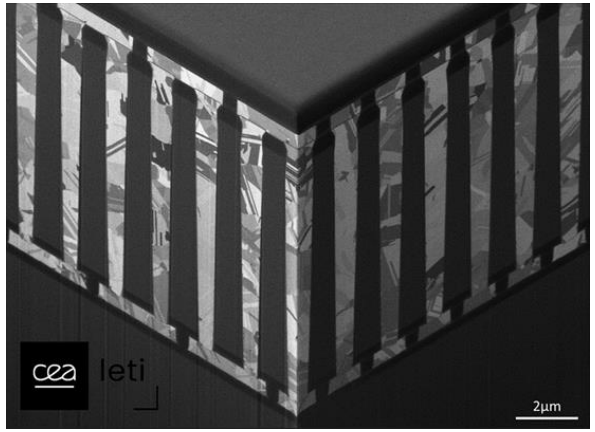
New through silicon vias

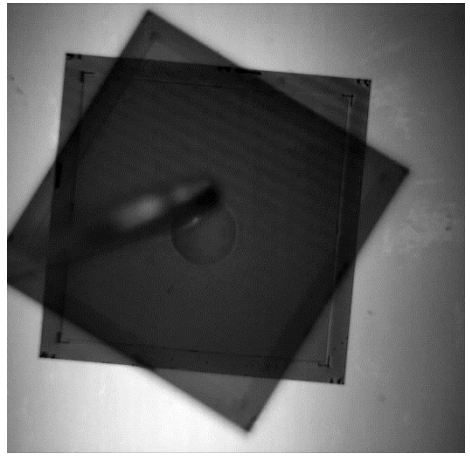
- Higher aspect ratio > 15
- Active or photonic interposers
- Warpage control layers

New manufacturing method

- Self assembly approach
- High throughput > 5000UPH
- Low cost



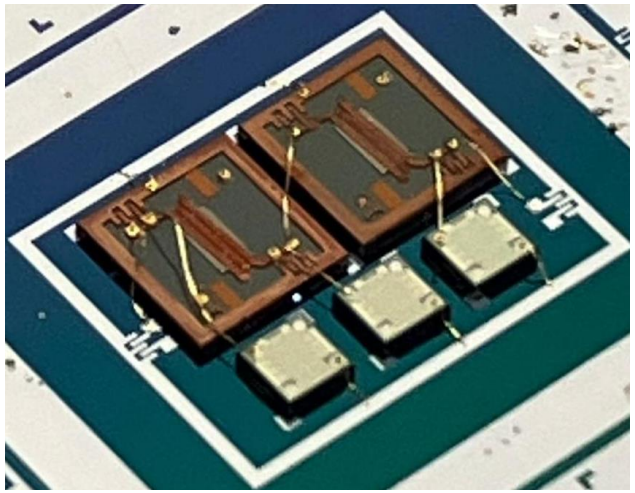




To increase interconnect density by a factor of up to 100

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Integrated Magnetics and PMIC for DC-DC power conversion



Power management integration in Systems-on-Chip

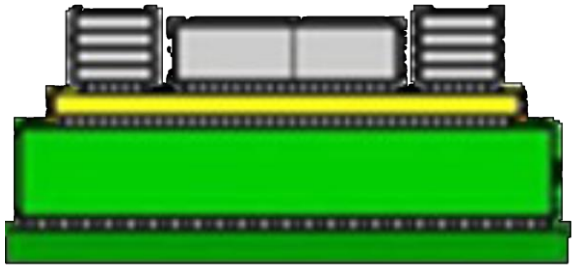
- Power converters densely co-integrated with digital or RF loading blocks
- Solutions to improve **power delivery** in chiplet architectures
- **Integration of passive components close to SOC**
- Design and fabrication of **integrated magnetics for inductive passive** components

FAMES will provide solutions to improve power delivery by integrating passive components into SOC

- Design and fabrication of integrated magnetics for inductive passive components
- Collective assembly of passives by Micro Transfer Printing (MTP)
- Performance assessments via a functional technology demonstrator that integrates an inductance-based DC-DC power converter, for granular power delivery

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

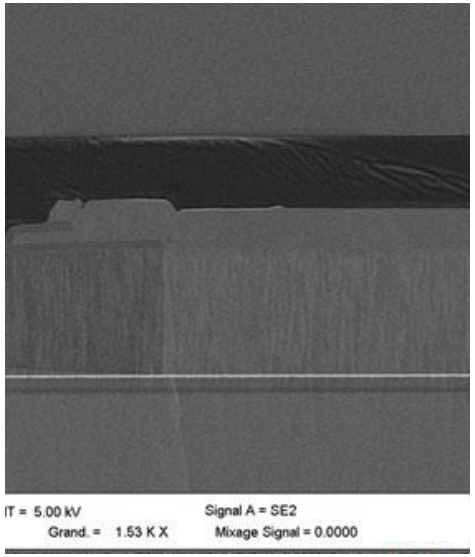
Power conversion: 3D caps



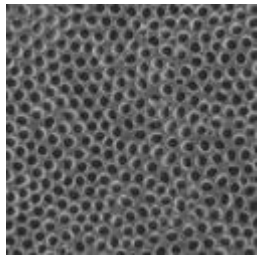
Hybrid integration

Hybrid integration of high density capacitors and CMOS power conversion stages on 300mm wafers for advanced 6G systems and HPC applications

- Very high density capacitors:
  - Specific ALD method developed for a MIM deposition with aggressive aspect ratios
  - TiN bottom and top electrodes
  - Si oxide and/or alumina for dielectrics



Higher surface capacitors



High A/R MIM

A game-changer for power signal management

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

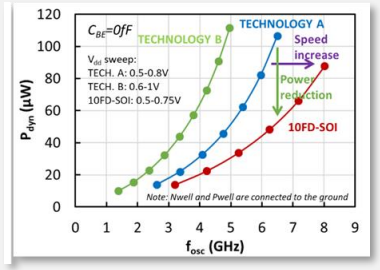
FAMES year 1 results highlights

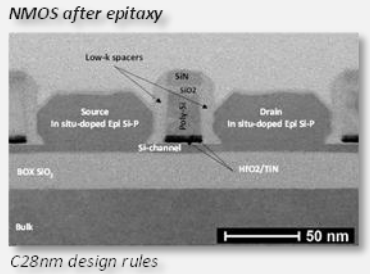
Infrastructure and procurement

- New cleanroom at CEA-Leti planned for delivery in 2025
- 24 pieces of equipment installed /15 ready for production

FD-SOI

- FD-SOI 10nm process assumptions ready for perf. evaluation
- First FD-SOI 10nm DRM and first GDS ready for tapeout
- Key process modules and FD-SOI10 architecture developed on relaxed pitch

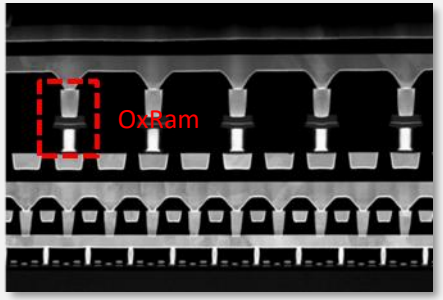


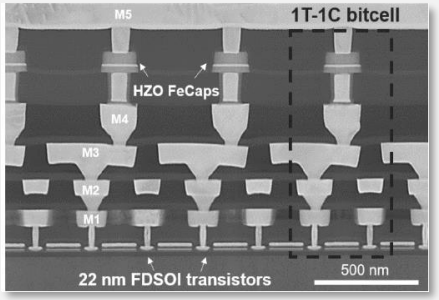


C28nm design rules

eNVM

- OxRAM 0.05 µm bit-cell tested
- FeRAM test vehicle characterized: **best state of the art** presented at IEDM2024
- Wafer scale MoS2 growth demonstrated

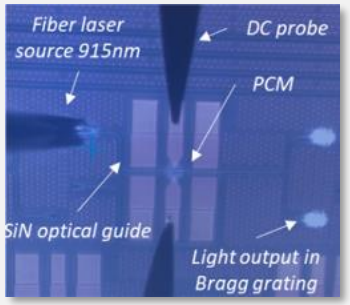


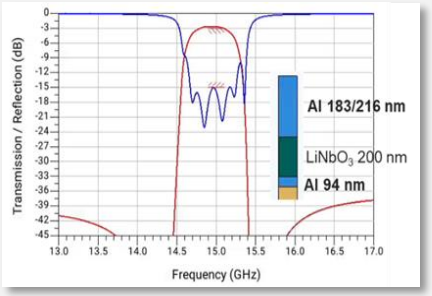


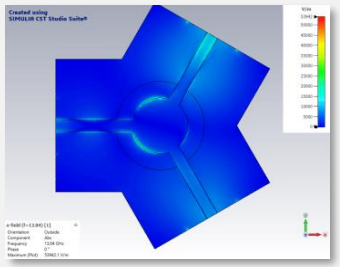
FAMES year 1 results highlights

RF components

- PCM RF switch with optical actuation (**world first**)
- FR3 $LiNbO_3$ filter design @15GHz
- FR3 and FR2-1 bands circulator design



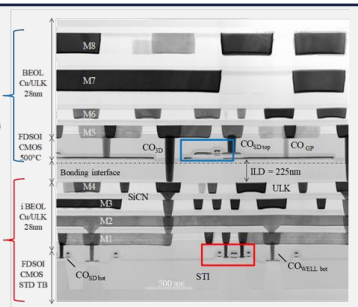




3D integration

- High density integrations (<5nm alignment) with sequential process
- Digital/RF 3D integration tested – cross talk analysis
- TSV process development for hybrid bonding integration

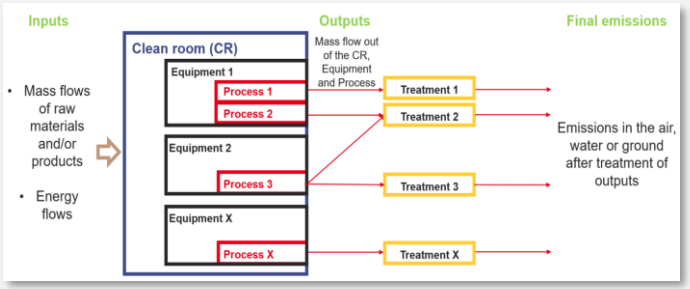
- Process flow & CMOS stack
  - FDSOI 28nm CMOS platform
  - 4 metal level Cu/ULK (28nm)
  - Ultra thin Inter Layer Dielectric (ILD)
  - Top channel and doped poly GP by bonding
  - FDSOI CMOS at 500°C
  - 3D contacts W/H = 100/450nm
  - 6 metal level Cu/ULK (28nm)



J. Lugo-Alvarez et al, VLSI 2024

Sustainability and environmental impact

- Life Cycle Assessment methodology
- E-score to introduce environmental KPI (PPAC-**E**)
- Cleanroom data collection platform



Accessing the FAMES Pilot Line

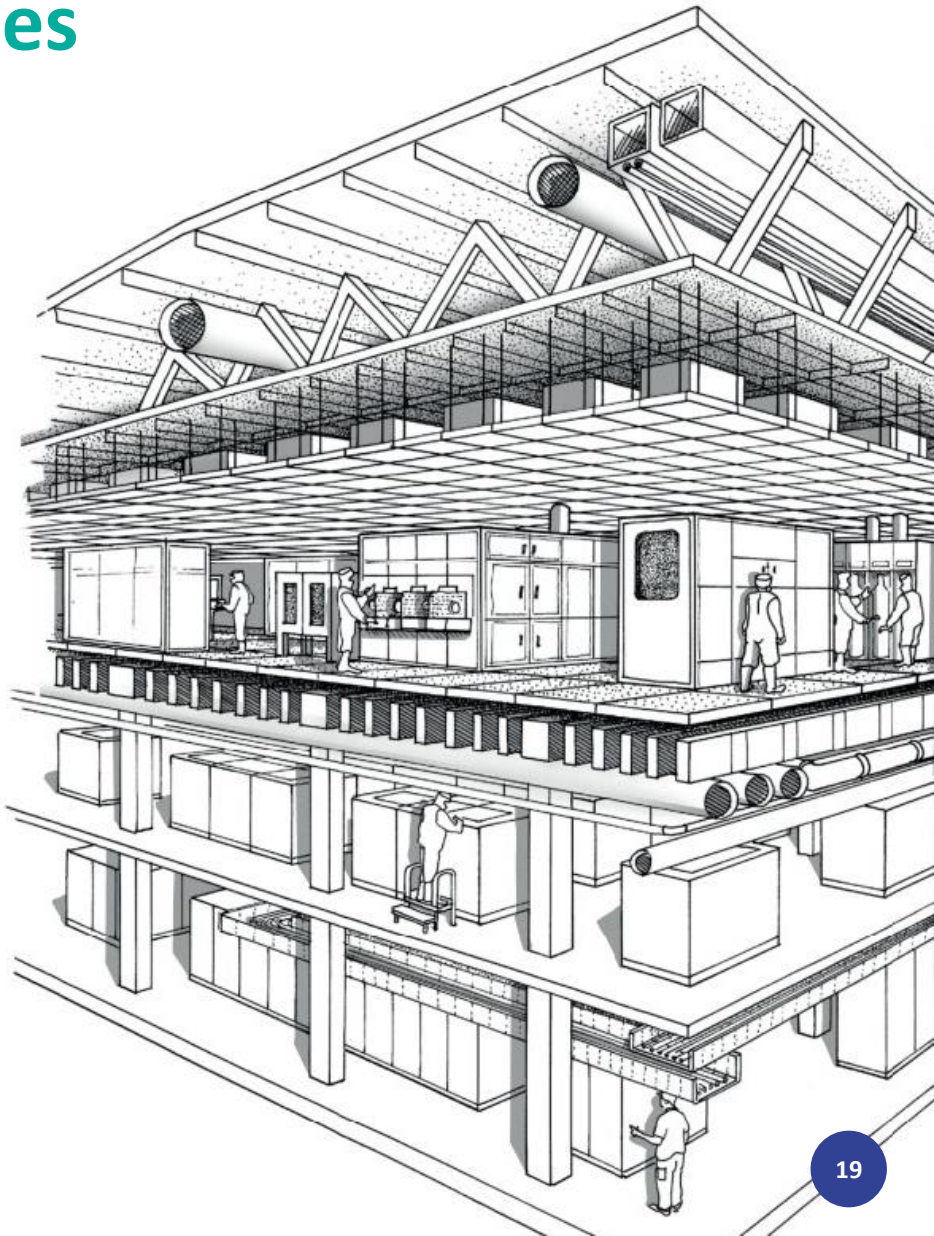
FAMES European open-access Pilot Line for advanced semiconductor technologies

Aim: Facilitate the adoption of FAMES Technologies to strengthen the European semiconductor ecosystem

To gain access to:

- Two types of PDKs (multi-project wafer or IC design assessment)
- The FAMES technologies (FD-SOI advanced nodes, embedded non-volatile memories, RF components, 3D integration options, PMIC) for performance evaluation
- Specific process steps, modules, integration flows, and demonstrator results
- Education and training on the FAMES technologies

as they become available



FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

The FAMES Pilot Line is open to all types of Users

LARGE COMPANIES

SMEs

START-UPs

RESEARCH COMMUNITY

Design Houses
Fabless
Foundries
Integrated Device Manufacturers
Material and Tool Suppliers
Universities
Research Centers

Two ways for Users to access the FAMES Pilot Line

Yearly Open-Access Calls
March to May

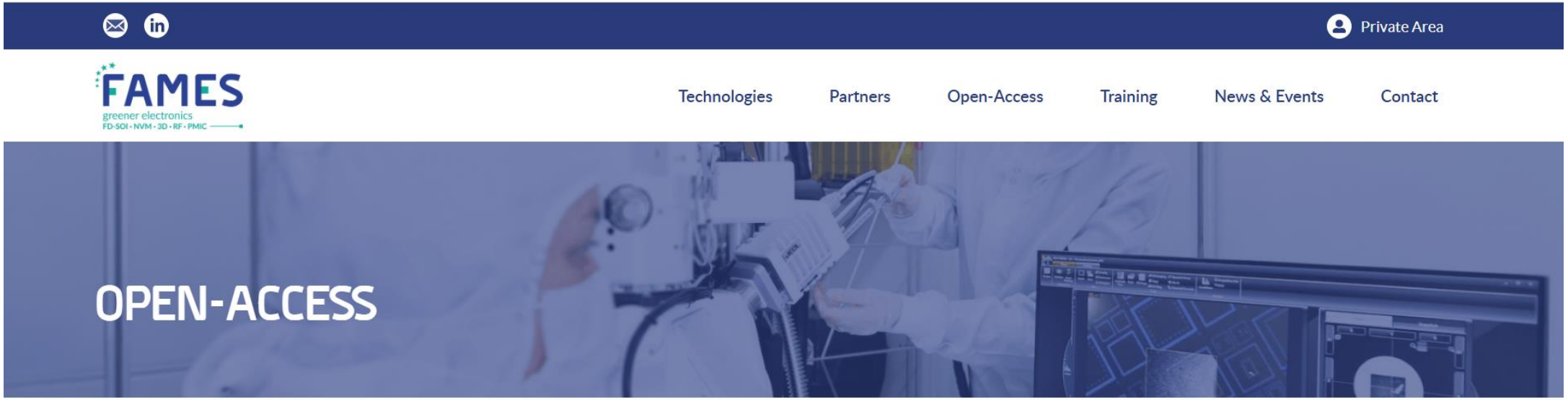
fames-pilot-line.eu

Spontaneous Requests
All year round

fames-pilot-line.eu

Competence centers and Design Platforms

Website: Open-Access page



FAMES Pilot Line

The FAMES Pilot Line offers European semiconductor stakeholders from industry, research, and academia **access to a unique slate of advanced semiconductor technologies**, chip design, testing, demonstrators and manufacturing capabilities.

This initiative aligns with the EU Chips Act to bolster the EU's semiconductor industry and support European technological sovereignty. Collaboration with other pilot lines in Europe will help build a tightly interconnected European chip ecosystem.

https://fames-pilot-line.eu/open-access/

FAMES

greener electronics

FD-SOI · NVM · 3D · RF · PMIC

(2023 – 2028)


cea
leti
Leti Innovation Days
June 17-19, 2025 | Grenoble, France
leti-innovation-days.com

Sponsors

The FAMES Pilot Line of the Chips JU is funded by Horizon Europe and Digital Europe Programs and the National Public Authorities of the partners involved. Grants N° 101182279 and 101182297.

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Thank you