The APECS pilot line – European chiplet innovation

Prof. Dr. Albert Heuberger

How APECS leads the way in heterogeneous integration by providing diverse design capabilities, technologies and testing strategies for electronic components and systems on a single platform

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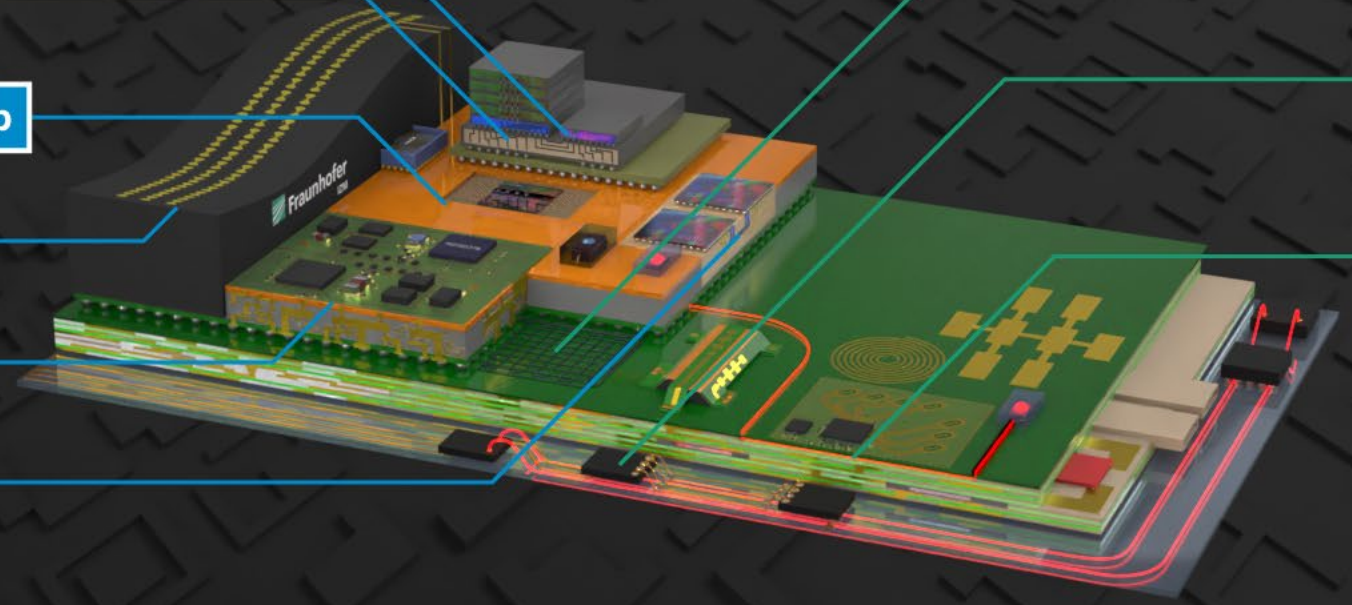
Examples for the integration at wafer and substrate level

Integration at wafer level

- Hybrid Cu/Cu bonds
- HDML Si-Interposer
- TF-embedded thin chip
- 3D-shaped mold cap
- TSV/TGV/TPV
- Embedded Si-bridge



Integration at substrate level

- Metallic TF-on-organic anti-tampering structures
- Embedded passives, chips or SiP module
- Embedded optical waveguides

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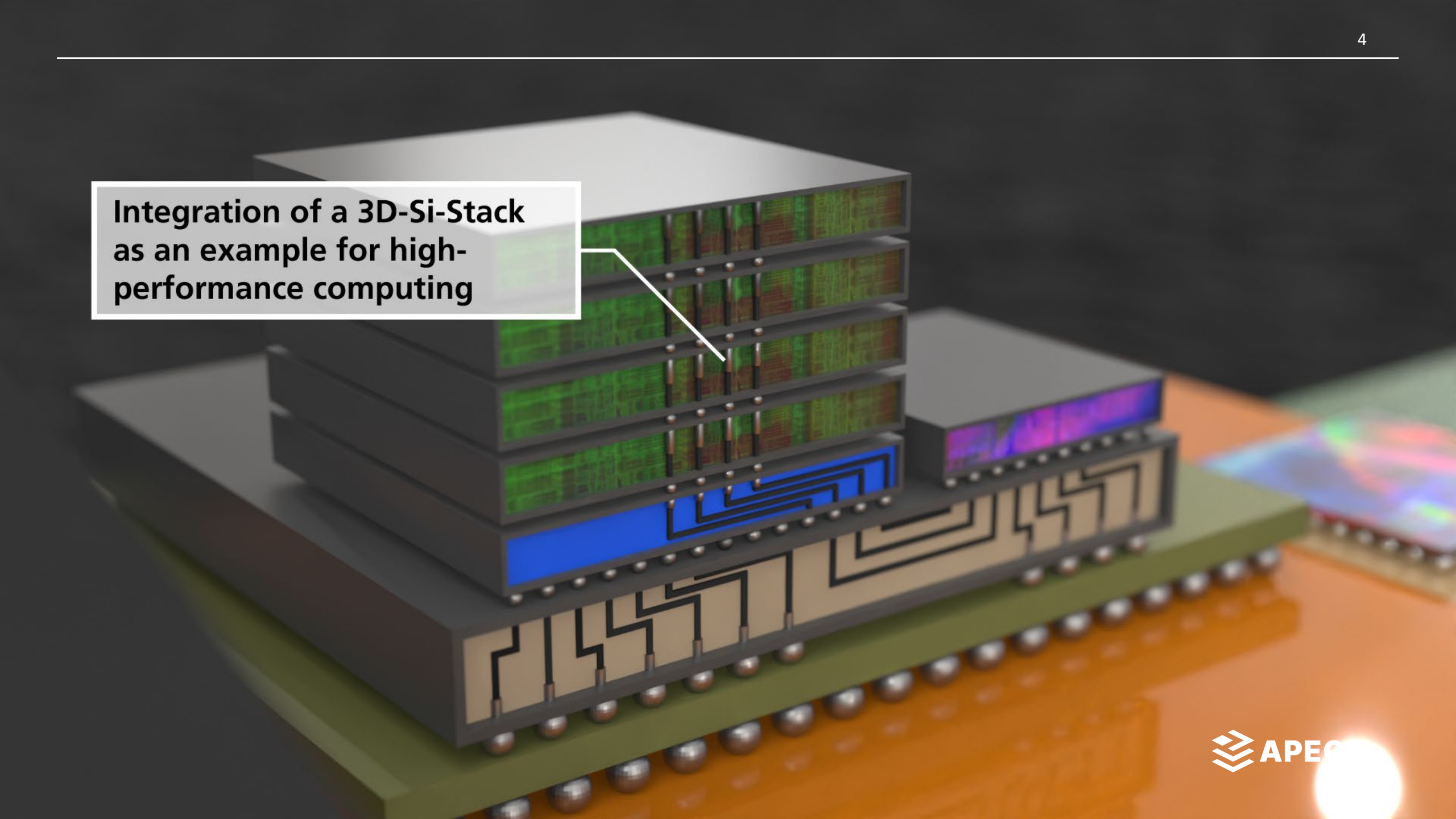
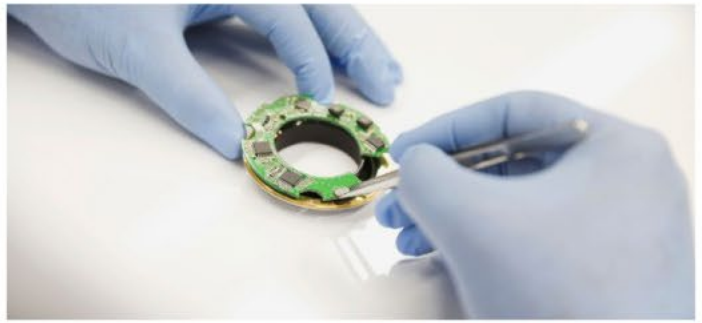

Integration of a 3D-Si-Stack
as an example for high-
performance computing

Application Aereas for Hetergenous Integration

High performance computing

Medical & scientific instrumentation

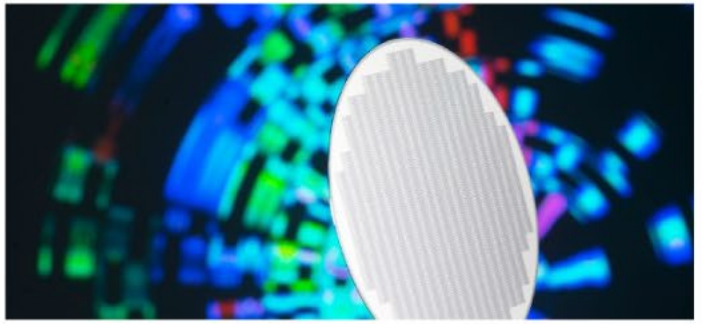


Sensor systems

Telecommunications

Industrial manufacturing

Artificial intelligence (AI / ML)



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What are the challenges in heterogeneous integration?

Design complexity

- Integrating different materials (CMOS, InP, GaAs, SiPh)
- Managing electrical and optical coupling
- Ensuring co-design efficiency and thermal stability

Standardization

- Defining universal design rules
- Standardizing interfaces
- Ensuring process compatibility
- Establishing reliability benchmarks

Manufacturing precision

- High density interposers (organic/inorganic)
- Sub-micron alignment
- Controlling process variations
- Enabling stress-free bonding
- New testing concepts

Cost management

- Reducing fabrication costs
- Improving yield
- Scaling automated assembly
- Minimizing supplier dependency

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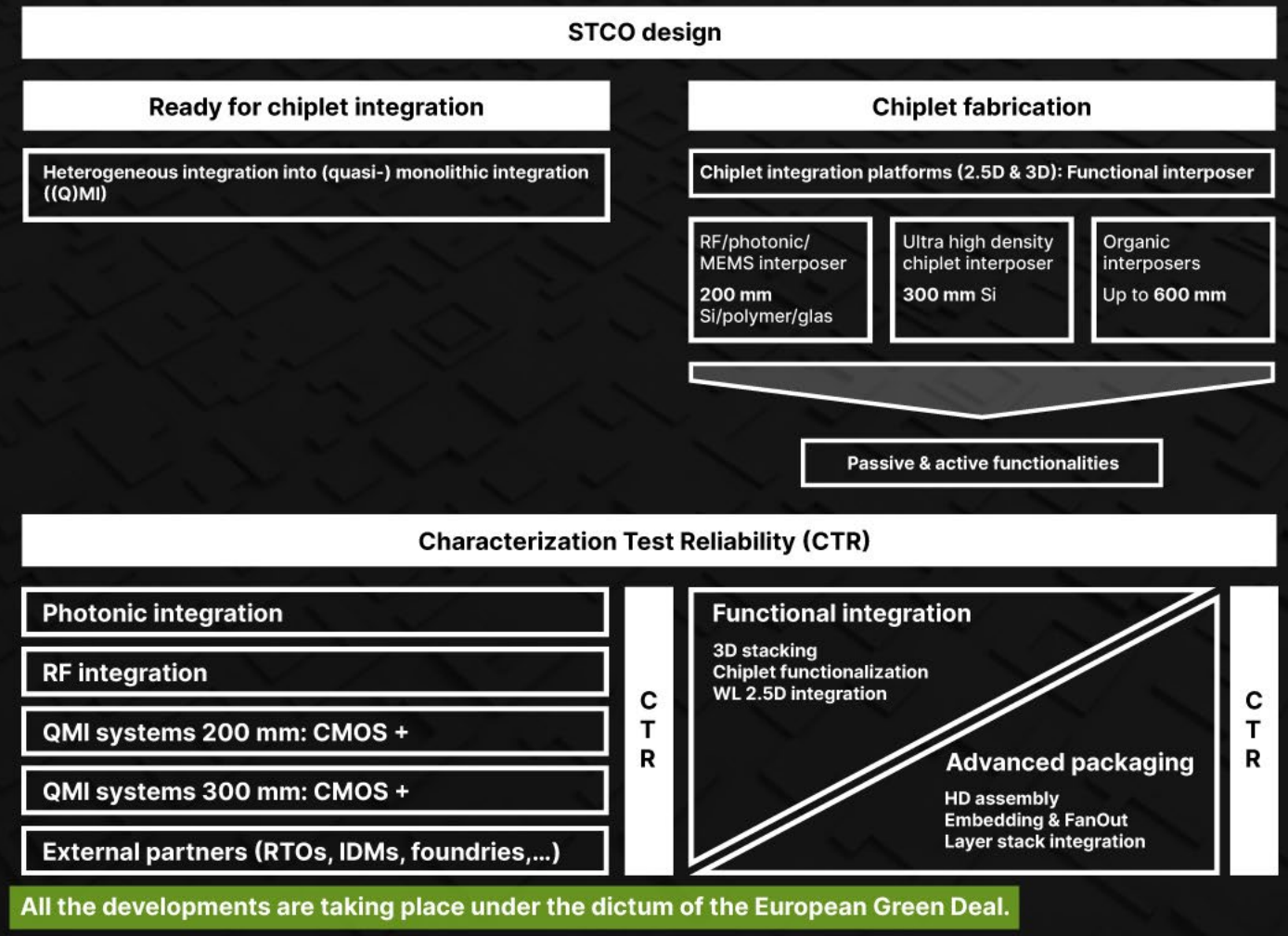
Purpose of the APECS pilot line

- Position **Europe´s R&D and industry at the forefront of semiconductor innovation**
- Establish a **cutting-edge infrastructure** for heterogeneous integration and chiplet technology
- Advance **technological capabilities for cutting-edge semiconductor devices**
- **Support European industries** (e.g., automotive, telecom, healthcare, IoT)
- **Join forces with Europe's RTOs** to accelerate technology transfer and enhance collaboration among

APECS brings the connection between design, technology and testing for wide range of applications



All the developments are taking place under the dictum of the European Green Deal.

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Key innovation of the APECS pilot line

1 Worldwide first **advanced automotive chiplet integration platform** (2.5D and 3D) for multiple core technologies (CMOS, Opto/RF) and non-electronic devices (MEMS, Opto, OLED), leveraging the innovations of advanced packaging

2 **Comprehensive end-to-end design flow and methodology** for chiplet-based advanced heterogeneous systems integration – Design-for-Performance, -Yield, -Power Efficiency, -Testability

3 Expansion of hetero-integration into **quasi-monolithic integration (QMI) for highest performance density** by leveraging Back-End-of-Line and Advanced Packaging capabilities

4 Prototyping of **high performance chiplet-based systems for specific needs of the European industries**, in particular, automotive, medical device and health care, sensors and advanced manufacturing industries

5 **Novel backend-of-line interfacing technology** for MEMS, opto/RF chips (III/V RF chiplets with (Bi)CMOS for 100 GHz+ frequencies)

6 **Novel testing concepts and technologies** for function-, quality- and yield- optimization

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Potential for industrial uptake

Users

- Chip Foundries
- Integrated Device Manufacturer (IDMs)
- Materials & Tools Supplier
- Semiconductor Customer
- Research Community
- Start-ups

Value Proposition

Design Services: enable chip, chiplet IP, and system design for APECS Pilot Line; provide and operate design platforms with support

Process development, materials and tool validation: accelerate technology development and validate processes for commercial transfer

System Development: leverage APECS tech for new products and business; enable access to specialized technologies

Manufacturing Outsourcing: offer Proof of Concept, prototype runs, small-volume production, and scalable transfer options

Design Services: enable chip, chiplet IP, and system design for APECS Pilot Line; provide and operate design platforms with support

Research Access: support research-to-application transfer; Provide easy access via local competence centers

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Central point of Contact

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Co-funded by

Chips JU

Co-funded by the European Union

Sponsored by the Federal Ministry of Education and Research

Freistaat Sachsen

Berlin

Bayerische Staatsregierung

SH Schleswig-Holstein Landesregierung

Baden-Württemberg

Die Landesregierung Nordrhein-Westfalen

Land Brandenburg

Sachsen-Anhalt

APECS is co-funded by the European Commission and national ministries of the eight member states within the framework of the EU Chips Act. Overall funding for APECS amounts to € 730 million over 4.5 years.

Ministry of Economic Affairs and Employment of Finland

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